What is claimed is:

1. In a semiconductor integrated circuit including: a hard macro having a plurality of combinational circuits for performing predetermined logic processing and a plurality of flip flops for performing data transfer, the hard macro being registered as a circuit pattern beforehand; an input flip flop for taking input data in synchronization with a clock signal; an output flip flop for outputting output data in synchronization with the clock signal; a first data path for giving the input data taken in the input flip flop to the hard macro; and a second data path for giving data outputted from the hard macro to the output flip flop,

the hard macro comprising:

a first flip flop for holding data given from the first data path at timing delayed from the clock signal,

a second flip flop for performing data transfer between the plurality of the combinational circuits in synchronization with the clock signal, and

a third flip flop for holding data outputted to the second data path at timing advanced from the clock signal for output.

2. The semiconductor integrated circuit according to claim 1, wherein the semiconductor integrated circuit has a delay device for delaying an external clock signal given from outside

and generating a clock signal given to the input flip flop and the output flip flop, and

the hard macro has an adjusting unit for adjusting timing of the external clock signal and feeding it to each of the first to third flip flops.

3. The semiconductor integrated circuit according to claim 1 comprising:

clock terminals for inputting a clock signal given to each of the first to third flip flops from outside, and

a clock wiring line for transmitting the clock signal inputted in each of the clock terminals to each of the first to third flip flops.

4. A semiconductor integrated circuit comprising:

a storage part for writing and reading data in synchronization with a timing signal;

an input flip flop for taking input data in synchronization with a clock signal;

an output flip flop for outputting output data in synchronization with the clock signal;

a first data path for giving the input data taken in the input flip flop to the storage part;

a second data path for giving data read out of the storage part to the output flip flop;

a timing supplying unit for giving a timing signal at timing delayed from the clock signal to the storage part when data is written in the storage part, and giving a timing signal at timing advanced from the clock signal to the storage part when data is read out of the storage part.